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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,721	09/30/2003	Frank Eliot Levine	AUS920030483US1	6347

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ART UNIT	PAPER NUMBER
2191	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,721	LEVINE ET AL.	
	Examiner	Art Unit	
	Ted T. Vo	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,9,10,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,9,10,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/30/07, 6/27/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the communication filed on 09/30/2003.

Claims 1-2, 9-10, 17-18 are pending in the application.

Response to Arguments

2. Response to Applicants' arguments:

- With regard to the terms' "indicator" in the claims which is addressed in the 112 second paragraph issue: As seen in the specification, there is no adequate description of "indicator". Applicants fail to point out the support in the specification. It is unclear to the meaning of "indicator" used in this specification. The Figures 3-4 in the specification mention "indicators", but it shows no descriptive information for the term, except instruction cache and performance monitor. For example, Figure 4: Performance indicator shadow cache.

In the Intel reference, It shows a performance monitor to identify bottle necks; it shows event counters to identify performance critical functions; or it is provided with event pointers to identify miss events cache miss, branch mispredicts, or TLB misses. The identifications of bottle necks, performance critical functions, miss events cache miss, branch mispredicts, or TLB misses, or so on, used for monitoring a performance of a program under Intel are interpreted as "indicator" of the claim.

In sec. 7, there are several processor instructions in which each instruction is used as a particular "indication". Therefore, Examiner interpreted "indicator" in that manner.

- With regard to the argument under 101 issue. The amendment fails to make the claims overcome under 35 USC 101. It should be note that a claim that is mere code/program/list/data structure per se is not a statutory claim. Claims 17-18 recite "A **computer program product in** a recordable-type computer readable medium". It is unclear the meaning of "product" in the claim; but according to the context of the claims, the term "product" which is in a computer readable medium should be program

code. It should be noted that claiming program code per se will be subjected under 101. It should be noted that "product" is known as being made by materials.

With regard to the argument under 102 issue.

Applicants alleged that Intel does not address the claims "identifying a routine that is used more than a threshold during execution of the program".

Examiner disagrees. Intel's teaching includes a program monitor associated with a processor. It monitors an execution of **a program**. See sec. 6.1.1.3, in p. 3 of sec. 6. It addresses "threshold", i.e. it discloses "identifying a routine that is used more than a threshold during execution of the program" – See statement: "By running a benchmark with different threshold values..." (p.3 of section 6). In light of the specification, the teaching of Intel does the same. It sets eight different values for thresholds. It should be noted that "benchmark" is a performance test of hardware and/or software. Examiner interprets a program/software are tested, for detecting a performance, by setting with different threshold values is an identified routine.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. The claims 17-18 are rejected under 35 U.S.C 101 because the claimed invention is directed to non-statutory subject matter.

As per claims 17-18: The claims recite "a computer program product" in which, within the scope of these claims, is data. For example, see the limitation that defines the scope of the claim: "A computer program product in a recordable-type computer readable medium". It is unclear the meaning of "product" in the claim. According to the context of the claims, the term "product" is code or programming instructions. It should be noted that claiming code per se is subject under 101. In this claimed subject

matter, the claims are limited to the code which is stored in a recordable-type medium. The scope of the claims is to claim the code per se. It should be noted that the meaning of "product" is thing that is being made by materials.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-2, 9-10, 17-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-2, 9-10, 17-18 recite the limitation, "indicators", where in the claims, this limitation is broadly and it has no adequate function/description for this limitation in the specification. the interpretation for "indicators" is the elements such as the segments of instructions in a program which cause "bottle neck", "cache miss", etc.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-2, 9-10, 17-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Intel, "Intel IA-64 Architecture Software Developer's Manual", Revision 1.1, Vol. 4, No. 245320-002, 7-2001.

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per Claim 1: Intel reference has 8 sections. Intel discloses,

A method in a data processing system for monitoring execution of instructions, the method comprising: executing a program (See Figure 6-2 in p. 4 of sec. 6);

Identifying a routine (i.e. a test program such as benchmark) ***that is used more than a threshold during execution of the program as a routine of interest*** (See sec. 6.1.1.3, particularly, see its second paragraph. Intel discloses an identifying of a routine such as a benchmark is tested with different threshold values for identifying the performance "knee");

responsive to identifying the routine of interest during execution of the program, dynamically associating instructions in the identified routine of interest with a set of performance indicators (sec. 6, p.7, i.e. triggers on events shown in table 6-2, see in the near end of the page, "registers indicate to...", see table 6.3, p. 10-11, and sec. 6, p. 13, "PMC/PMD register assignments for each monitoring feature...") ***to form a modified routine*** (See sec. 6, p. 5, "are interesting identifying performance bottlenecks and relating them back to their source code": *identifying a routine of interest during execution of a program; then see "code instrumentation", in p. 26 of sec 6*), ***wherein the set of performance indicators comprises one of a set of performance indicators located in a field within the instruction*** (See Figure 6-5, that detects indicators as instructions instrumented in the IA-64 instruction execution. These instructions are seen in sec. 7, such as instruction PIPELINE_FLUSH. Also see "performance monitor events , event counters, seen in sec. 6.1.2.2, and 6.1.2.3, p. 3, or program counter sampling for identifying hot spot, see in sec. 6, p.6) ***and a set of performance indicators located in a shadow memory*** (Each of instructions shown in the sec. 7 is associated with associated with event code, and registers such as PMC/PMD (See table 6.3, p. 10-11, and sec. 6, p. 13, "PMC/PMD register assignments for each monitoring feature..."), ***and wherein the set of performance indicators identify***

that the instructions are to be monitored; (For example, monitoring cache; or see sec. 6.2.2 for setting maximum per-cycle event increment, etc); ***and***

responsive to execution of an instruction in the modified routine (i.e. the routine contains hotspot results by profiling) ***during continued execution of the program, incrementing a counter*** (i.e., the performance counters. For example, see sec. 6, Figure 6-5, p. 7), ***wherein the counter provides a value identifying a number of times that the instruction in the modified routine is executed*** (e.g. sec. 6.2.2, p.16 of sec. 6).

As per Claim 2: Intel discloses, ***The method of claim 1 further comprising: associating instructions in a second routine of interest with a second set of indicators to form a second modified routine*** (Intel discloses a program that has many routines, and each of routine in monitored)***; and responsive to execution of an instruction in the second modified routine, incrementing a second counter*** (See sec. 6, Figure 6-5, p. 7).

As per Claims 9-10: See rationale addressed in the rejection of claims 1-2 above.

As per Claims 17-18: See rationale addressed in the rejection of claims 1-2 above.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

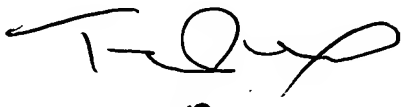
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708.

The facsimile number for the organization where this application or proceeding is assigned is the Central Facsimile number **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TTV
February 14, 2007



TED VO
PRIMARY EXAMINER